

SECRET

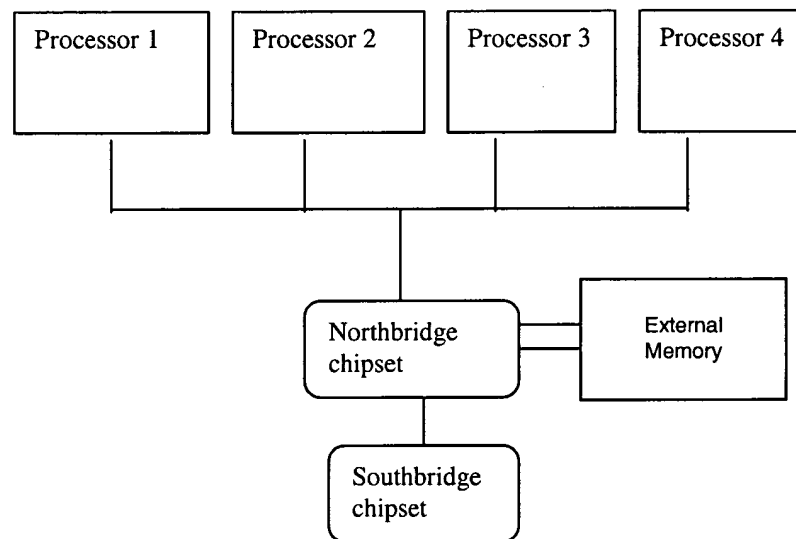


Figure 1

200

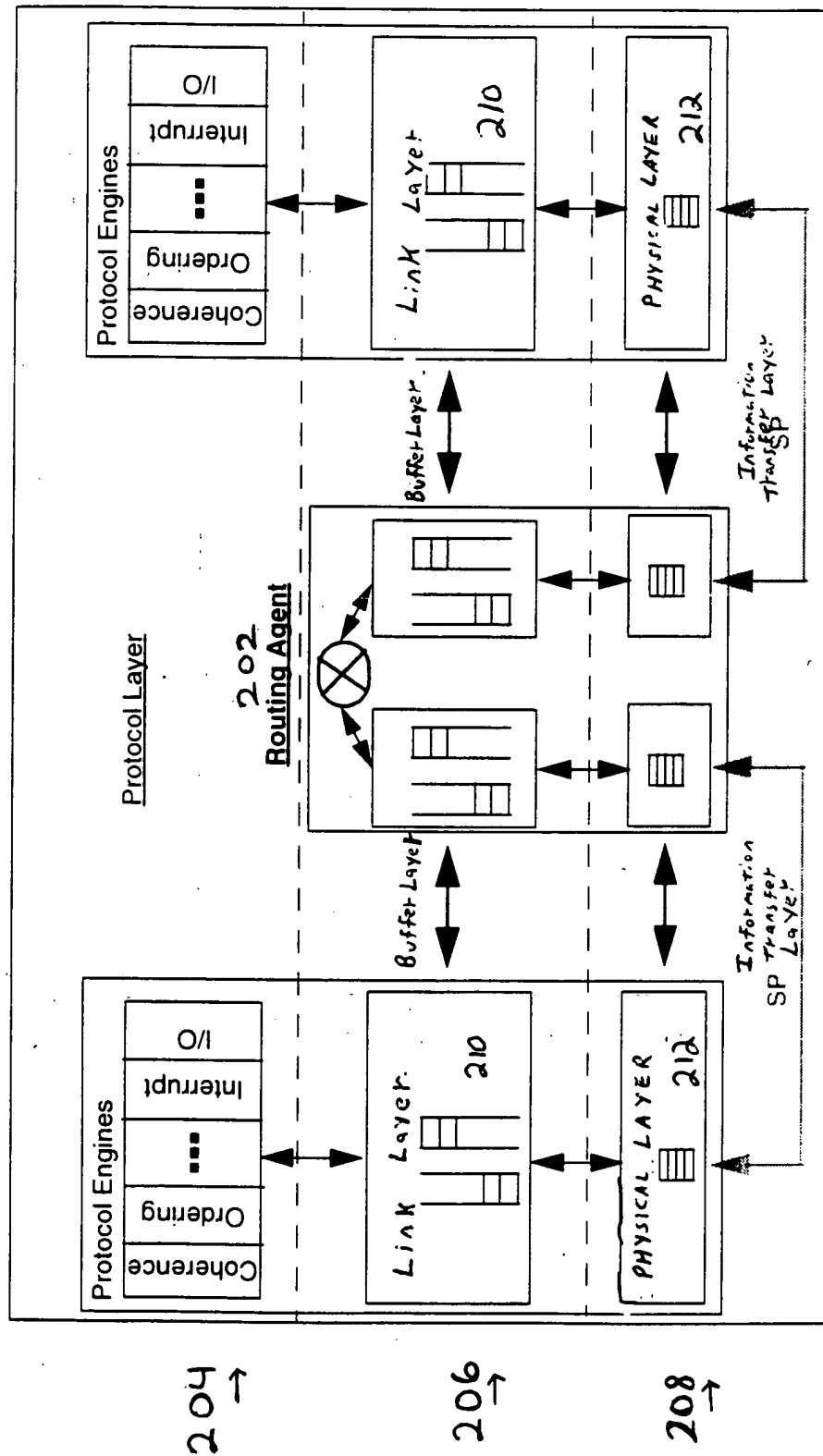


Figure 2

48 bit

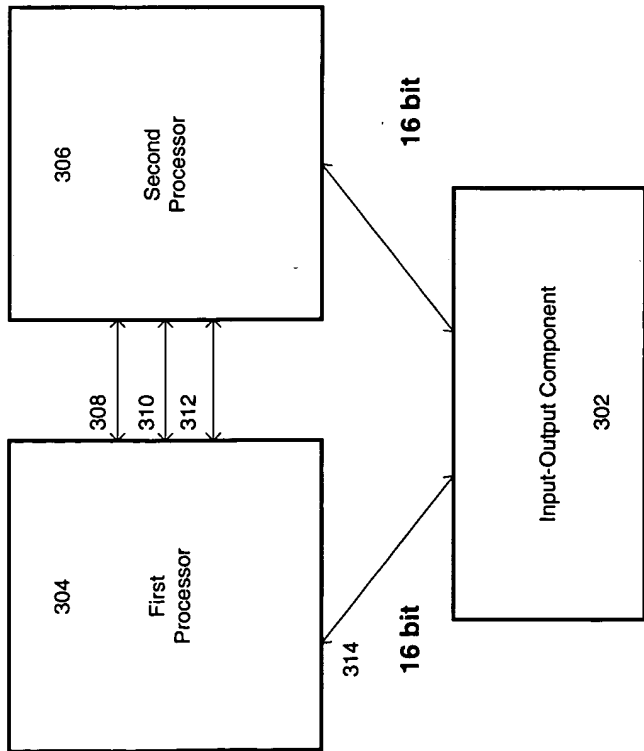


Figure 3

32 bit

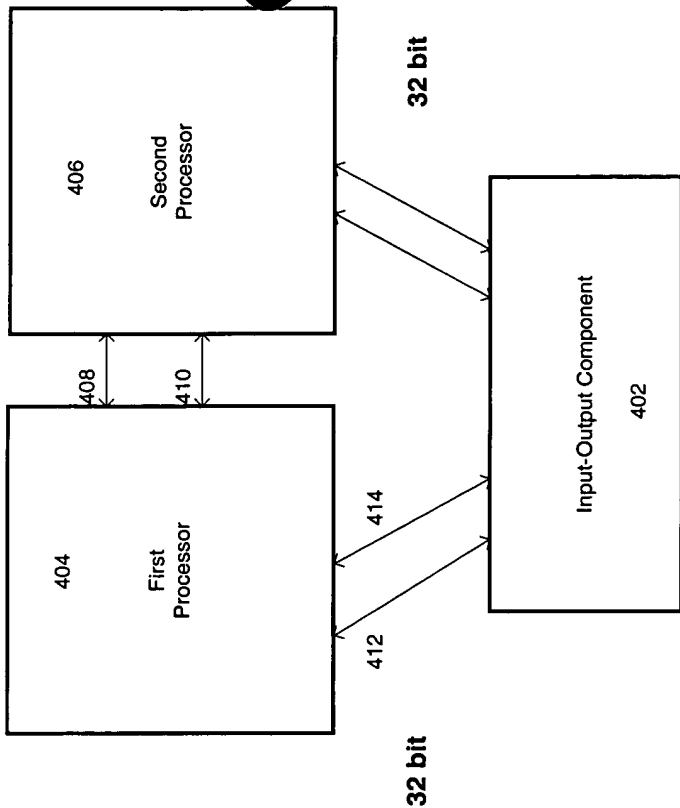


Figure 4

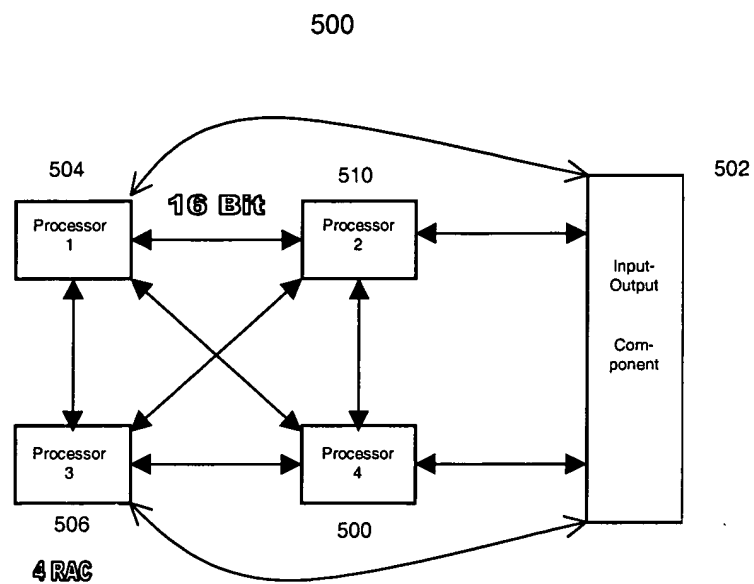
[illegible]

Figure 5

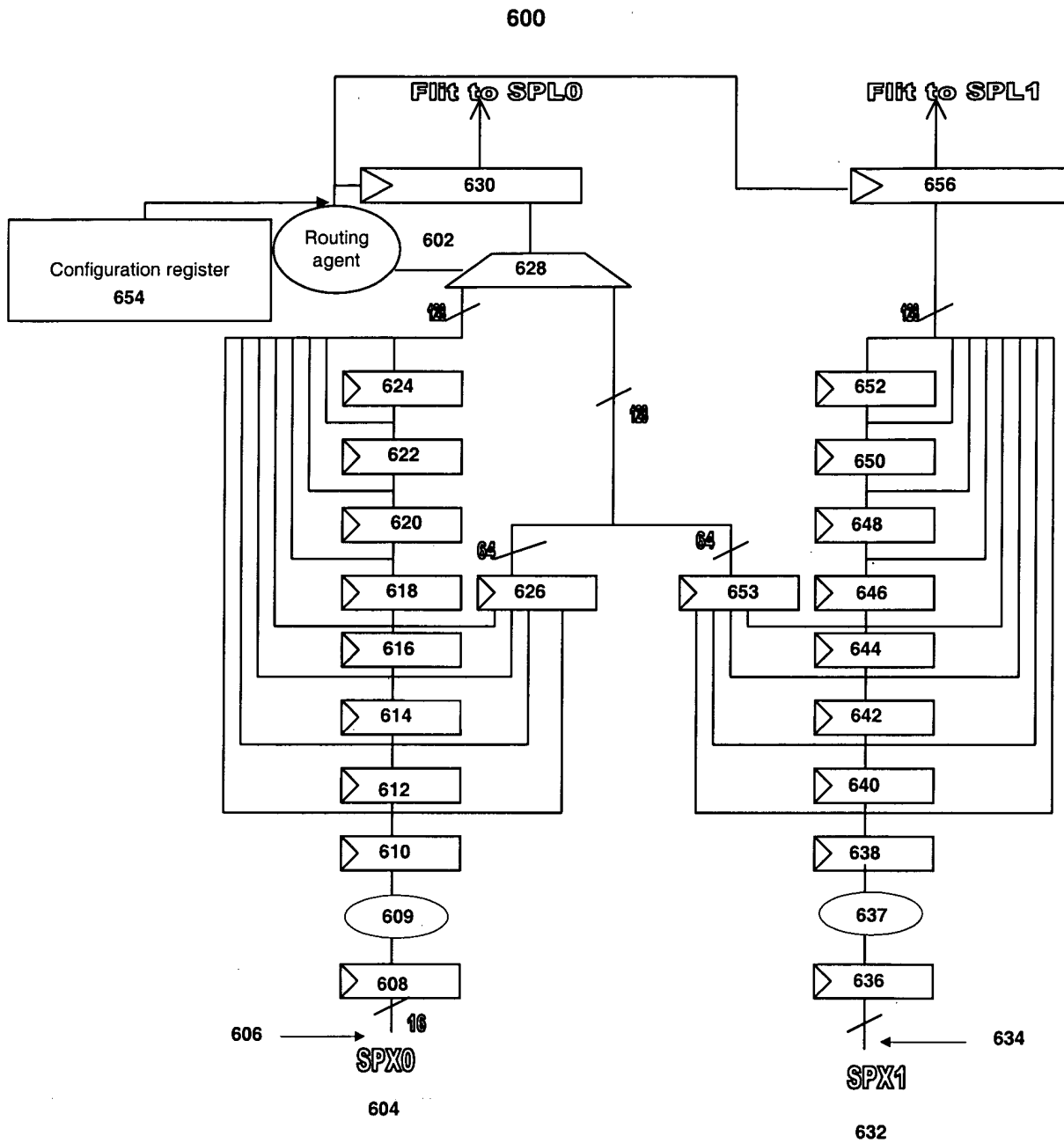


Figure 6

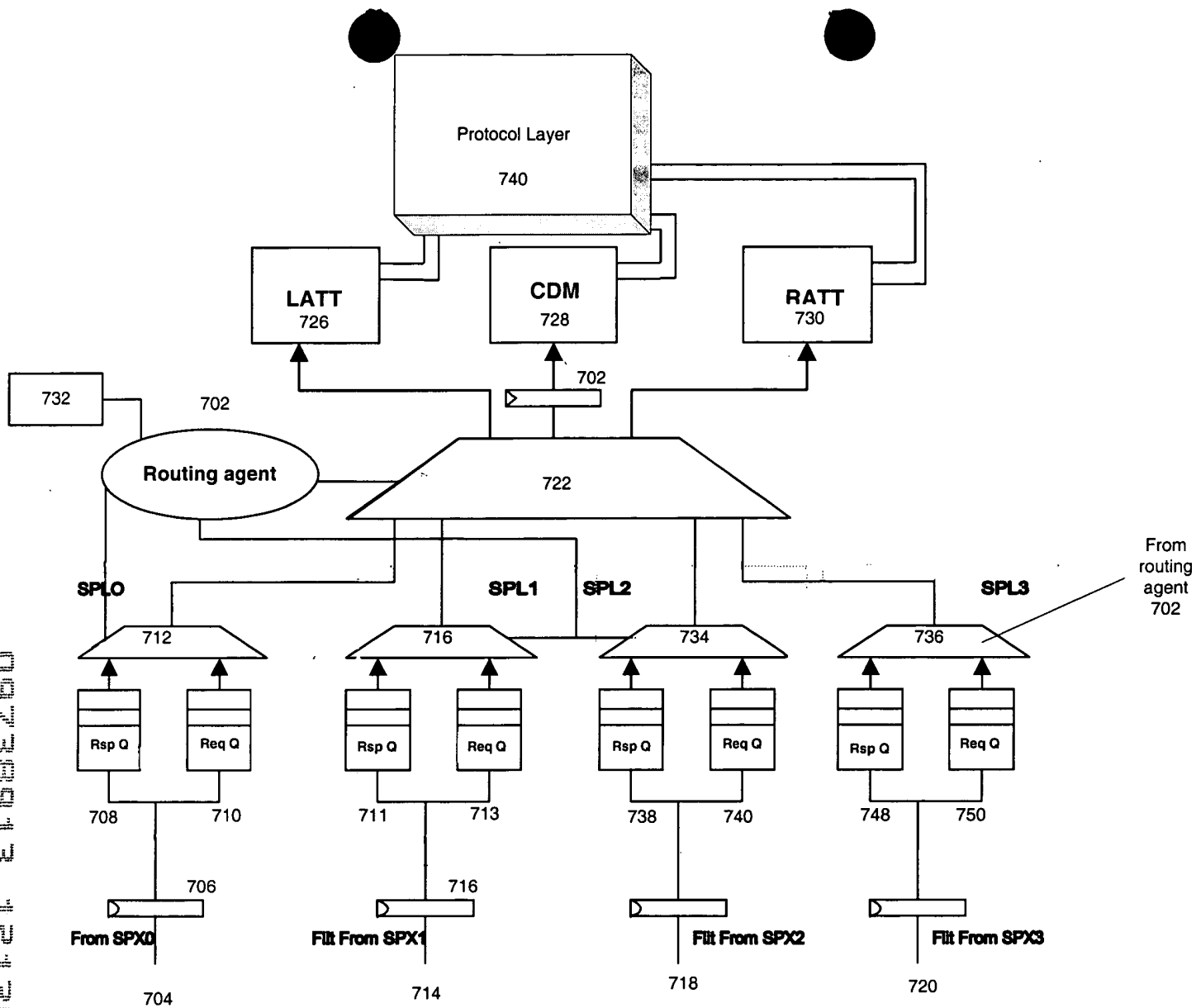


Figure 7

The diagram illustrates a dual-path system architecture, labeled 931 and 932. Each path starts with three input queues: Request Queue (Req Q), Response Queue (Rsp Q), and Retransmission Queue (Retry Q). These inputs feed into a series of multiplexers and registers.

- Path 931:** The inputs feed into a first multiplexer (908) which outputs to register 910. This register feeds into another multiplexer (912) which outputs to register 911. Register 911 feeds into a third multiplexer (916) which outputs to register 920. Register 920 feeds into a fourth multiplexer (926) which outputs to register 927. Register 927 feeds into a fifth multiplexer (928) which outputs to the Routing Agent (902). The Routing Agent (902) also receives input from component 924 and outputs to component 904. Component 904 feeds back into the first multiplexer (908).
- Path 932:** Similar to Path 931, but it lacks the Routing Agent (902) and component 904. Instead, the output of the fifth multiplexer (934) feeds directly into a sixth multiplexer (930) which outputs to component 906.

Clock signals are provided to various components in both paths:

- "Read from Q's at 100/200 based on 16/32 BK Link" feeds into the first multiplexers (908 and 934).
- "Clock at 200/400 based on 16/32 Link" feeds into registers 912 and 916 in Path 931, and their counterparts in Path 932.
- "Clock at 400/800 based on 16/32 Link" feeds into registers 920 and 927 in Path 931, and their counterparts in Path 932.

Data flow widths are indicated by numbers along the connections: 64, 32, 16, and 800A.

Figure 9